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TRANSMITTAL OF APPEAL BRIEF (Large Entity)

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In Re Application Of: Jack A. Mandelman, et al.

Serial No.
10/004,152

Filing Date
10/24/2001

Examiner
David S. Blum

Group Art Unit
2813

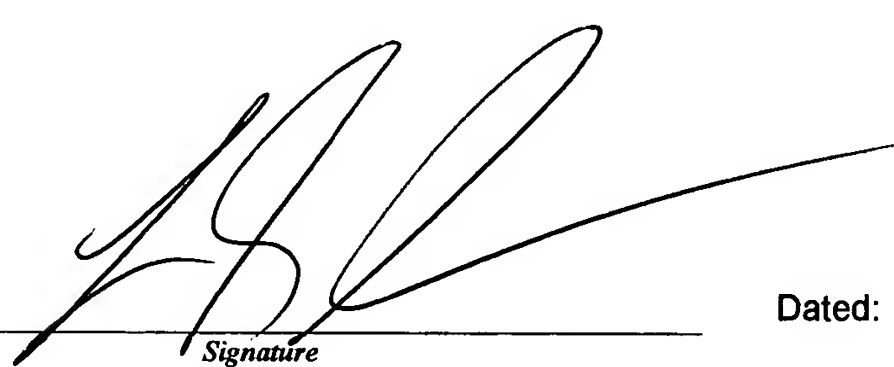
Invention: **METHOD FOR MULTI-DEPTH TRENCH ISOLATION**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on

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Dated: May 17, 2004

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Jack A. Mandelman, et al. **Examiner:** David S. Blum

Serial No: 10/004,152

Art Unit: 2813

Filed: October 24, 2001

Docket: FIS920010265US1 (14912)

For: METHOD FOR MULTI-
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Dated: May 17, 2004

Confirmation No.: 8522

Commissioner for Patents
P.O. Box 1450
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APPELLANTS' BRIEF ON APPEAL UNDER 37 C.F.R. § 1.192

1. Real Party in Interest

The real party in interest of the present application is International Business Machines Corporation, the assignee of the entire right, title and interest in the above-identified patent application. The assignment to International Business Machines Corporation from the inventors has been recorded on October 24, 2001 at Reel 012362, Frame 0644.

2. Related Appeals and Interferences

No other appeals or interferences are known which directly affect, or will be directly affected by, or have a bearing on, the disposition of the pending appeal.

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3. Status of the Claims

The present application was filed on October 24, 2001 with Claims 1-20; Claim 1 is a first independent claim to which Claims 2-11 are dependent on, and Claim 12 is a second independent claim to which Claims 13-20 are dependent on. The originally filed claims are all directed to methods of forming multi-depth apertures (Claims 1-11) or multi-depth isolation regions (Claims 12-20) in a substrate.

In a Response dated September 5, 2002 to a first Office Action that issued on June 5, 2002, amendments to Claims 1 and 12 were made. A second Office Action finally rejecting Claims 1-20 issued on November 4, 2002, to which appellants filed a Request for Continued Examination (RCE) on February 4, 2003. The RCE submission included an Amendment and Response wherein Claims 1 and 12 were amended for a second time.

In the RCE, a first Office Action was issued on February 25, 2003. Appellants responded to the first Office Action in the RCE by submitting a Response dated May 27, 2003. None of the claims were amended in that submission. A Final Rejection in the RCE application was issued on November 17, 2003. A 116 Response, including argumentation only, was filed on January 20, 2004. Despite the arguments made in Appellants' 116 Response, the Examiner issued an Advisory Action dated February 19, 2004. A Notice of Appeal, with a one-month extension of time, was filed on March 17, 2004.

Thus, Claims 1-20, of which only Claims 1 and 12 have been amended during the prosecution of this case, are the subject of this appeal. The claims as they presently stand are set forth in the Appendix of this Appeal Brief. The status of each of the claims on appeal is as follows:

Claims 1-20 are finally rejected and are on appeal.

4. Status of the Amendments

A Response under 37 C.F.R. § 1.116 to the Final Rejection dated November 17, 2003 including arguments for patentability only was filed on January 20, 2004. Appellants' Response under 37 C.F.R. § 1.116 was considered and entered by the Examiner.

5. Summary of the Invention

The invention embodied by Claims 1-11, on appeal, relates to a method for forming a plurality of apertures in a substrate, each aperture having a predetermined depth, wherein at least two of the apertures have different depths. See Page 1, lines 8-11 and Page 3, lines 14-16. In accordance with the embodiment set forth in Claims 1-11, the method begins with providing a pad stack 12 atop a surface of a substrate 10 having regions, e.g., Regions 1, 2 and 3, for forming apertures 30, 28, and 24, respectively. This step of the present invention is described at Page 6, line 9-Page 8, line 3 and is shown, for example, in FIG 1. In accordance with the present invention, the pad stack 12 includes at least a top patterned masking layer 20 that exposes portions of the pad stack 12. The top patterned masking layer 20 serves as the *single critical mask* used in the present invention in defining apertures in the substrate 10. See Page 6, lines 14-16 and FIG 2. Next, at least one of the regions (e.g., Regions 1 and 2) of the substrate 10 is blocked with a first block mask 22, while leaving at least one other region (e.g., Region 3) of the substrate 10

unblocked. This step of Claim 1, on appeal, is described at Page 8, lines 18-25 and is illustrated, for example, in FIG 3.

A plurality of first apertures 24 having a first depth d_1 are formed in the unblocked region (e.g., Region 3) of the substrate 10 using the patterned masking layer 20 to define the plurality of first apertures 24 by first removing the exposed portions of the pad stack 12 to expose portions of the substrate 10 abutting the patterned masking layer 20 and then removing the exposed portion of the substrate 10. This step of the method recited in Claim 1, on appeal, is described at Page 8, line 27-Page 9, line 7 and is shown, for example, in FIG 4. As is shown, in FIG 4, the first apertures 24 have sidewalls that are aligned to outer edges of the top patterned masking layer 20.

Next, the first block mask 22 is removed, as described at Page 9, lines 5-7, and a plurality of second apertures 28 having a second depth d_2 are formed in regions (e.g., Region 2) of the substrate 10 that were previously blocked by the first block mask 22 using the patterned masking layer 20 to define the second apertures 28, while simultaneously increasing the first depth d_1 such that d_1 is greater than d_2 . This step of the claimed invention, on appeal, is described at Page 9, lines 9-23 and is shown, for example, in FIGS 5 and 6. As also shown in FIG 5, the second apertures 28 have sidewalls that are aligned to outer edges of the top patterned masking layer 20 which are formed by first removing said exposed portions of the pad stack 12 to expose portions of the substrate 10 abutting the patterned masking layer 20 in Region 2 and then removing the exposed portion of the substrate 10.

Further processing as described at Page 9, line 25-Page 10, line 4 can be performed to form additional apertures 30 in the other regions of the substrate, e.g., Region 1. See, also, FIGS 7-8.

Insofar as the method of Claims 12-20, on appeal, are concerned, the processing steps recited in Claim 12, on appeal, are nearly identical to those mentioned above, except that the apertures are defined as trench isolation regions. This embodiment recited in Claims 12-20, on appeal, represents a preferred embodiment of the instant application. See, for example, Page 1, lines 11-14, Page 3, lines 18-20, and Page 5, lines 1-2, lines 14-16, and lines 25-28.

6. Issues on Appeal

I. Do the combined disclosures of U.S. Patent No. 5,298,845 to Verret (hereinafter “Verret”) and U.S. Patent No. 6,207,534 to Chan, et al. (hereinafter “Chan, et al.”) render Claims 1-3, 5-14 and 16-20, on appeal, unpatentable?

II. Do the combined disclosures of Verret, Chan, et al. and U.S. Patent No. 6,150,212 to Divakaruni, et al. (hereinafter “Divakaruni, et al.”) render Claims 4 and 15, on appeal, unpatentable?

7. Grouping of the Claims

The claims involved in the two issues on appeal all stand or fall together.

8. Arguments for Patentability

I. The combined disclosures of Verret and Chan, et al. do not render Claims 1-3, 5-14 and 16-20, on appeal, unpatentable.

This rejection relies on the combined disclosures of Verret and Chan, et al. for allegedly disclosing the claimed method recited in Claims 1-3, 5-14 and 16-30, on appeal. Appellants respectfully disagree with the Examiner's position that the foregoing disclosures render Claims 1-3, 5-14 and 16-20, on appeal, obvious. In the present claims, on appeal, a method is provided which includes *forming a plurality of apertures (or first trench isolation regions) having a first depth in an unblocked region of a semiconductor substrate using a patterned masking layer to define the plurality of first trench isolation regions by first removing exposed portions of a pad stack to expose portions of the substrate abutting the patterned masking layer and then removing the exposed portion of the substrate; and thereafter forming a plurality of second apertures (or trench isolation regions) having a second depth in regions of the semiconductor substrate that were previously blocked by a first block mask using the patterned masking layer to define the second aperture (or trench isolation regions).*

In accordance with the present methods recited in Claims 1 and 12, on appeal, and during the forming of the second apertures (second trench isolation region), the first depth of the first apertures (first trench isolation regions) is increased at the same time as formation of the second apertures (second trench isolation regions) such that the first depth is deeper than the second depth. The second apertures (trench isolation regions) are formed by first removing the exposed portions of the pad stack to expose portions of

the substrate abutting the patterned masking layer and then removing the exposed portion of the substrate.

Thus, in the claimed methods, the first and second apertures (and first and second trenches) have sidewalls that are aligned to outer edges of the top patterned masking layer. In the claimed methods, *the top patterned masking layer is employed as a single critical mask that is used in defining each of the apertures*. The use of a single critical mask to define sets of apertures of different depths is *not* disclosed in any of the art cited in the Office Action dated November 17, 2003.

Verret discloses a method which includes the steps of depositing a SiN layer 34 and a first photoresist layer on a surface of substrate 30 which includes SiO₂ layer 32 formed thereon; patterning the first photoresist layer to provide a patterned photoresist 36 which has openings that expose SiN layer 34; etching the exposed SiN layer and removing the first photoresist layer; forming a second photoresist layer 42 having opening 44 on the now patterned SiN layer; etching a first trench 46 into the substrate through opening 42; removing the second photoresist layer; and etching to provide second trench 52 while deepening the first trench.

In Verret, a first masking layer 36 is required to pattern the SiN layer 34, and neither the first masking layer 36, nor the patterned SiN layer 34 is used to define the first trench or aperture, as is required in the claimed methods. Instead, a second patterned photoresist 42 is used in defining the first trench. As a consequence, in the prior art disclosure, the first trench has sidewalls that are aligned with the second photoresist, not the patterned SiN layer 34. In Verret, the second photoresist is used as the critical mask in defining the first trench.

Appellants respectfully submit that in Verret the second trench as well as the upper portion of the first trench have sidewalls that are aligned to the patterned SiN layer 34; the lower portion of the first trench disclosed in Verret does not have sidewalls aligned to the patterned masking layer 34.

Appellants thus submit that in Verret *two different critical masks; second photoresist 42 and patterned SiN layer 34*, are used in defining the trenches. In the claimed methods, on appeal, however, the first and second apertures (or first and second trench isolation regions) are formed using the same critical mask. As a consequence, the sidewalls of the first and second apertures (or first and second trench isolation regions) provided in the claimed methods, on appeal, have sidewalls that are aligned with the outer edges of the top patterned masking layer.

Chan, et al. do not alleviate the above defects in Verret since the applied secondary reference also does not teach or suggest appellants' claimed methods which include the processing steps recited in the claims, on appeal. Chan, et al. provide a method of forming trenches having different depths. In accordance with the process disclosed in Chan, et al., the different trench depths are formed by depositing an oxide layer overlying a silicon substrate; etching through the oxide layer to the top surface of the silicon substrate to form openings for planned first trenches; depositing a polysilicon layer overlying the oxide layer and filling the openings for the planned first trenches; polishing down the polysilicon layer to the top surface of the oxide layer such that the polysilicon layer remains only in the openings of the planned first trenches; thereafter etching through the oxide layer to the top surface of the silicon substrate to form openings for planned second trenches; *etching simultaneously the silicon substrate*

and the polysilicon to complete the first trenches and the second trenches, wherein the etching forms second trenches deeper than first trenches; and completing the fabrication of the integrated circuit device.

In accordance with the process disclosed in Chan, et al., different trench depths are formed into the Si substrate during *a single etching step*, See FIG. 9. This is achieved in the prior art by providing a placeholder material of polysilicon 42 in a predetermined position on the surface in which the first trenches are to be formed, while exposing other areas of the substrate in which second trenches are to be formed. During the etching step, the polysilicon and Si substrate, which are both exposed, are simultaneously etched using chemistry that selectively removes silicon. The depth of the trenches is controlled by the absence, or presence, of the polysilicon layer 42. See Col. 4, lines 15-16.

This is different from the claimed invention, on appeal, in which *a plurality of apertures (or trench isolation regions) having different depths are formed using the same critical mask using different etching steps*. Appellants respectfully submit that the combination of Verret and Chan, et al. would utilize a method of forming different depth trenches using the technique disclosed in Chan, et al.

Appellants further submit that the rejection under 35 U.S.C. § 103 also fails because there is no motivation in the applied references which suggests modifying the disclosed methods to include the various features mentioned and highlighted above. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above.

In the absence of motivation to modify the methods disclosed in Verret and Chan, et al., the prior art references do not render the claims, on appeal, obvious. See In re Vaeck, 947 F.2d 488, 493, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991).

In view of the various reasons articulated herein, it is respectfully submitted that the combined disclosures of Verret and Chan, et al. do not render Claims 1-3, 5-14, and 16-20, on appeal, obvious under 35 U.S.C. § 103.

II. The combined disclosures of Verret, Chan, et al. and Divakaruni, et al. do not render Claims 4 and 15, on appeal, unpatentable.

This rejection relies on the combined disclosures of Verret, Chan, et al. and Divakaruni, et al. for allegedly disclosing the claimed feature recited in Claims 4 and 15, on appeal. The specific feature is that the patterned masking layer employed in independent Claims 1 and 12 is a silicate glass selected from boron doped phosphorus silicate glass and tetraethylorthosilicate. Appellants respectfully disagree with the Examiner's position that the foregoing disclosures render Claims 4 and 15, which are dependent on Claims 1 and 12, respectively, on appeal, obvious.

Appellants respectfully submit that for this obviousness rejection the combination of Verret and Chan, et al. is defect for the same reasons mentioned above. Hence, the above arguments made in Section I of this brief are incorporated in this section by reference. To reiterate: the combined disclosures of Verret and Chan, et al. do not teach or suggest the processing steps recited in Claims 1 and 12, on appeal. Particularly, the applied references do not teach or suggest *forming a plurality of apertures (or first trench isolation regions) having a first depth in an unblocked region of a semiconductor substrate using a patterned masking layer to define the plurality of first trench isolation*

regions by first removing exposed portions of a pad stack to expose portions of the substrate abutting the patterned masking layer and then removing the exposed portion of the substrate; and thereafter forming a plurality of second apertures (or trench isolation regions) having a second depth in regions of the semiconductor substrate that were previously blocked by a first block mask using the patterned masking layer to define the second aperture (trench isolation regions).

The above defects in the combined disclosures of Verret and Chan, et al. are not alleviated by the disclosure of Divakurani, et al. Appellant respectfully submit that Divakaruni, et al., is further removed from the claimed method than either Verret or Chan, et al. as evident by the fact that the Examiner has relied on Divakaruni, et al. for disclosing the types of patterned masking layers defined in dependent Claims 4 and 15, on appeal. Appellants find no disclosure in Divakaruni, et al. that teaches or suggests using a patterned masking layer to define a first trench, and thereafter a second trench, wherein the first trench is deeper than the second trench. As such, the combination of Verret, Chan, et al. and Divakaruni, et al. does not render appellants' claimed method obvious.

The § 103 rejection citing the combination of Verret, Chan, et al. and Divakaruni, et al. also fails because there is no motivation in the applied references which suggests modifying the methods disclosed therein to include appellants' claimed processing steps. This rejection is thus improper since the prior art does not suggest this drastic modification. The law requires that a prior art reference provide some teaching, suggestion, or motivation to make the modification obvious.

Here, there is no motivation provided in the disclosures of the applied prior art references, or otherwise of record, which would lead one skilled in the art to modify the methods of the applied references to include appellants' claimed sequence of processing steps recited in Claims 1 and 12, on appeal, that lead to the formation of apertures (or trenches) of different depths using a single critical mask. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 972 F.2d, 1260,1266, 23 USPQ 1780,1783-84 (Fed. Cir. 1992).

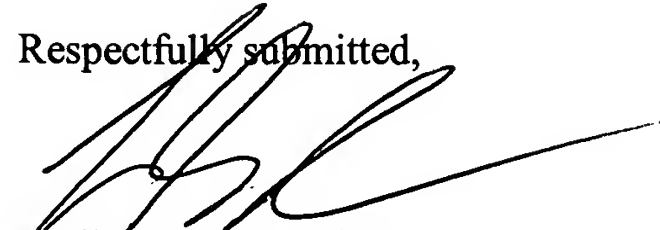
In view of the various reasons articulated herein, it is respectfully submitted that the combined disclosures of Verret, Chan, et al. and Divakaruni, et al. do not render Claims 4 and 15, on appeal, obvious under 35 U.S.C. § 103.

9. Conclusion

The above arguments establish that all of the claims, on appeal, are patentable over the combined disclosures of Verret and Chan, et al. as well as the combined disclosures of Verret, Chan, et al., and Divakurani, et al. Appellants therefore respectfully request that the final rejection under 35 U.S.C. §103 citing the foregoing

references made in the Office Action dated November 17, 2004 be reversed by the Board of Patents Appeals and Interferences.

Respectfully submitted,



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APPENDIX

10. The claims on appeal for U.S. Application Serial No. 10/004,152, filed October 24, 2001

1. (Previously Amended) A method for forming multi-depth apertures in a substrate comprising the steps of:

(a) providing a pad stack atop a surface of a substrate having regions for forming apertures therein, said pad stack including at least a top patterned masking layer that exposes portions of said pad stack, said top patterned masking layer serving as the single critical mask used in defining apertures in said substrate;

(b) blocking at least one of said regions of said substrate with a first block mask, while leaving at least one other region of said substrate unblocked;

(c) forming a plurality of first apertures having a first depth in said unblocked region of said substrate using said patterned masking layer to define said plurality of first apertures by first removing said exposed portions of said pad stack to expose portions of said substrate abutting said patterned masking layer and then removing said exposed portion of said substrate, said first apertures having sidewalls that are aligned to outer edges of the top patterned masking layer;

(d) removing said first block mask; and

(e) forming a plurality of second apertures having a second depth in regions of said substrate that were previously blocked by said first block mask using said patterned masking layer to define said second apertures, while simultaneously increasing said first depth such that said first depth is deeper than said second depth, said second

apertures having sidewalls that are aligned to outer edges of the top patterned masking layer which are formed by first removing said exposed portions of said pad stack to expose portions of said substrate abutting said patterned masking layer and then removing said exposed portion of said substrate.

Claim 2. (Original) The method of Claim 1 wherein said substrate is a semiconductor substrate, a conductor, an insulator or mixtures and multilayers thereof.

Claim 3. (Original) The method of Claim 1 wherein said pad stack further includes a pad oxide layer and a pad nitride layer, wherein said pad nitride layer is formed atop said pad oxide layer.

Claim 4. (Original) The method of Claim 1 wherein said patterned masking layer is a silicate glass selected from the group consisting of boron doped phosphorus silicate glass and tetraethylorthosilicate.

Claim 5. (Original) The method of Claim 1 wherein said patterned masking layer is formed by deposition, lithography and etching.

Claim 6. (Original) The method of Claim 1 wherein said first block mask includes a first photoresist layer.

Claim 7. (Original) The method of Claim 1 wherein said plurality of first apertures and said plurality of second apertures comprise openings, trenches, grooves, notches, holes, slits, gaps, slots, clefts, vias, voids, passages or mixtures thereof.

Claim 8. (Original) The method of Claim 1 wherein said plurality of first apertures and said plurality of second apertures are formed by etching.

Claim 9. (Original) The method of Claim 1 wherein said etching comprises reactive-ion etching.

Claim 10. (Original) The method of Claim 1 further comprising blocking additional portions of said substrate with a second block mask prior to conducting step (e); conducting step (e); removing said second block mask; and forming a plurality of third apertures having a third depth, while simultaneously increasing the first and second depths such that the first depth is greater than the second depth, which is greater than the third depth.

Claim 11. (Original) The method of Claim 10 further comprising the steps of repeating blocking and forming a plurality of apertures in each previously blocked region such that different sets of apertures are formed in said substrate, each set having different depths associated therewith.

12. (Previously Amended) A method of forming multi-depth isolation regions in a semiconductor substrate comprising the steps of:

(a) providing a pad stack atop a surface of a semiconductor substrate having regions for forming trench isolation regions therein, said pad stack including at least a top patterned masking layer that exposes portions of said pad stack, said top patterned masking layer serving as the single critical mask used in defining trenches in said substrate;

(b) blocking at least one of said regions of said semiconductor substrate with a first block mask, while leaving at least one other region of said semiconductor substrate unblocked;

(c) forming a plurality of first trench isolation regions having a first depth in said unblocked region of said semiconductor substrate using said patterned masking layer to define said plurality of first trench isolation regions by first removing said exposed portions of said pad stack to expose portions of said substrate abutting said patterned masking layer and then removing said exposed portion of said substrate, said first trench isolation regions having sidewalls that are aligned to outer edges of the top patterned masking layer;

(d) removing said first block mask; and

(e) forming a plurality of second trench isolation regions having a second depth in regions of said semiconductor substrate that were previously blocked by said first block mask using said patterned masking layer to define said second trench isolation regions, while simultaneously increasing said first depth such that said first depth is deeper than said second depth, said second trench isolation regions having sidewalls that

are aligned to outer edges of the top patterned masking layer which are formed by first removing said exposed portions of said pad stack to expose portions of said substrate abutting said patterned masking layer and then removing said exposed portion of said substrate.